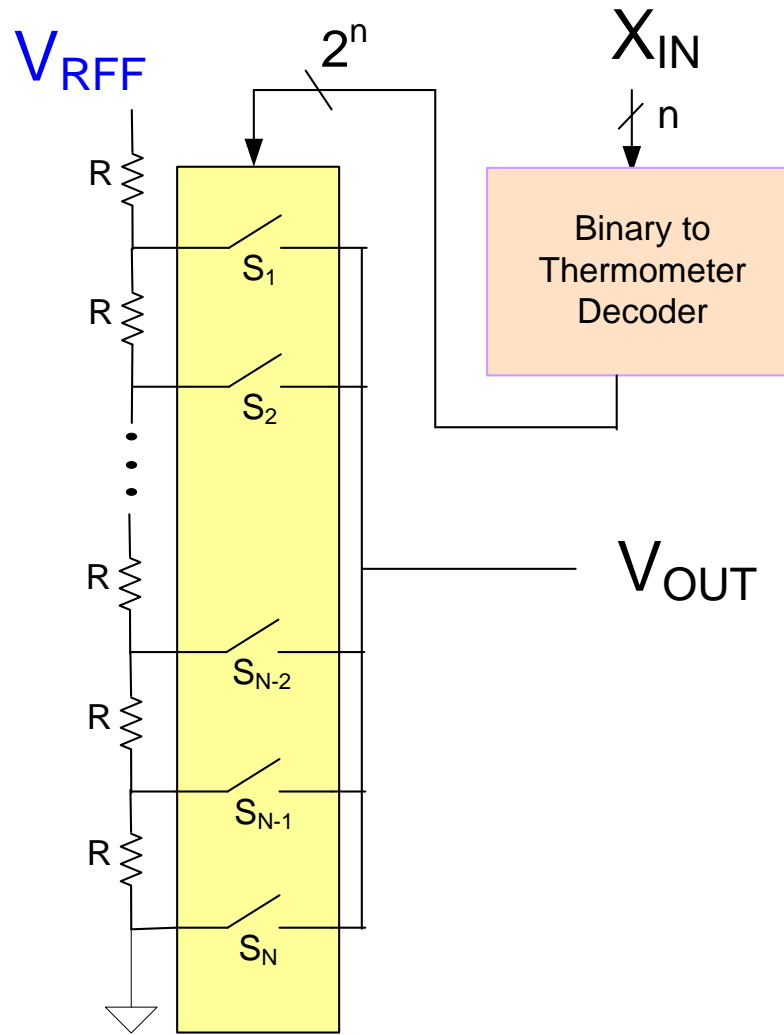# EE 435

Lecture 32

- Switch Implementation
- Current Steering DACs
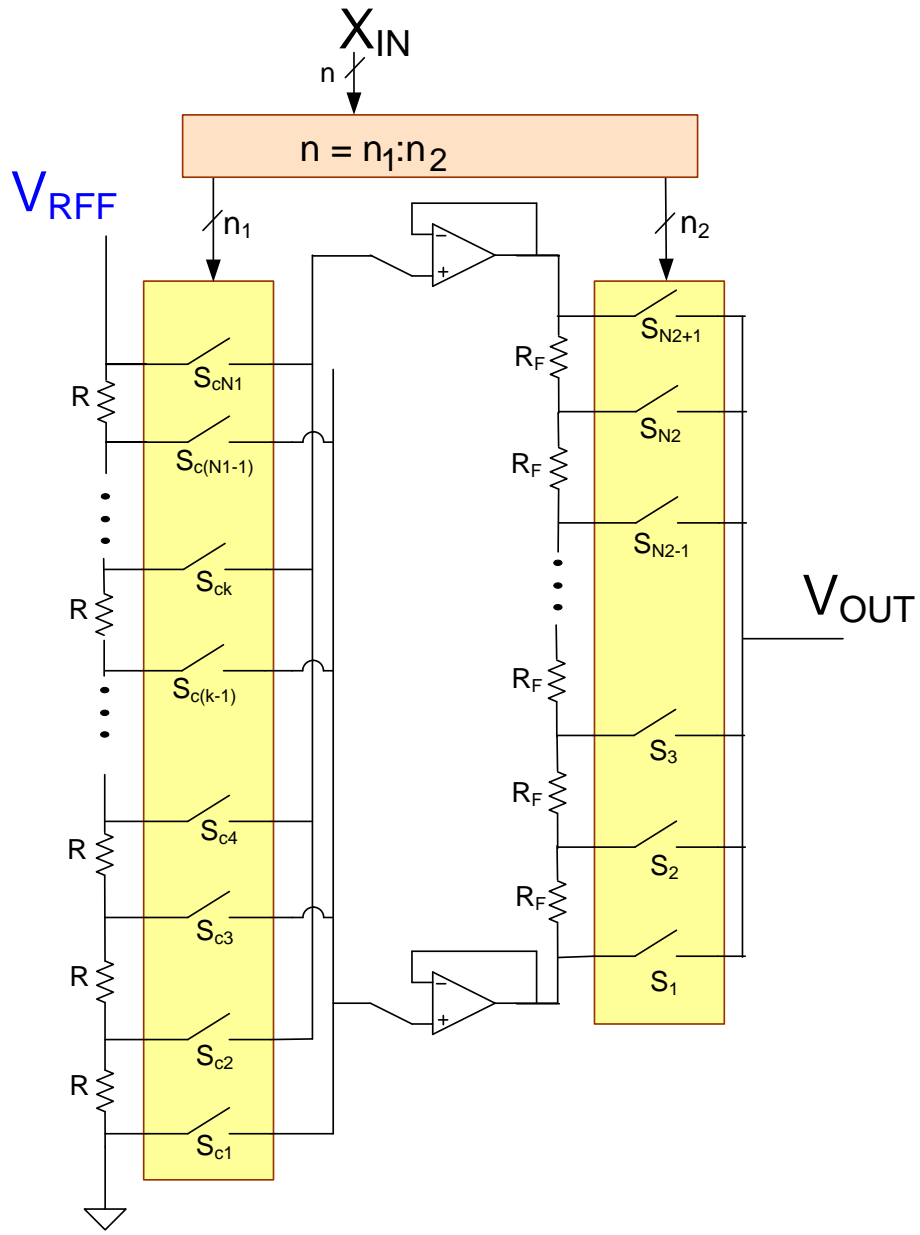
R-String DAC
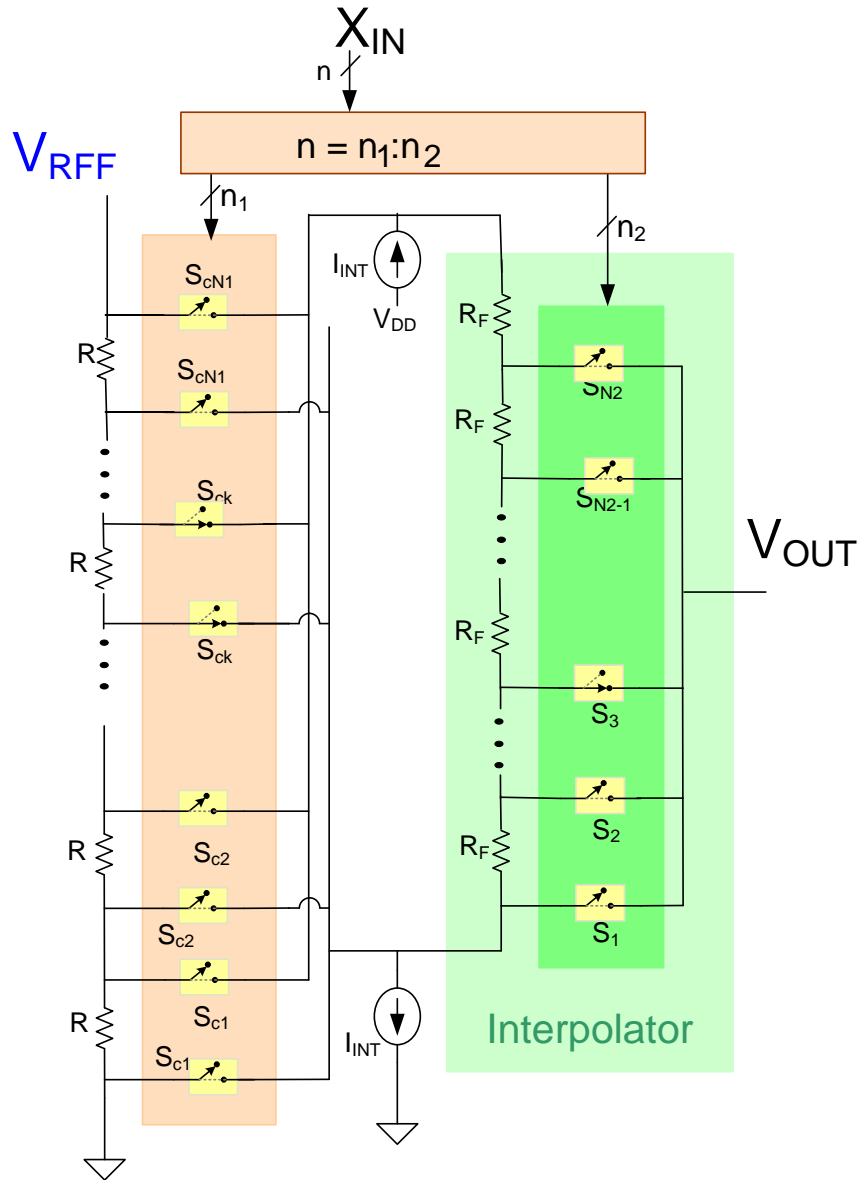

Basic R-String DAC including Logic to Control Switches

R-String DAC

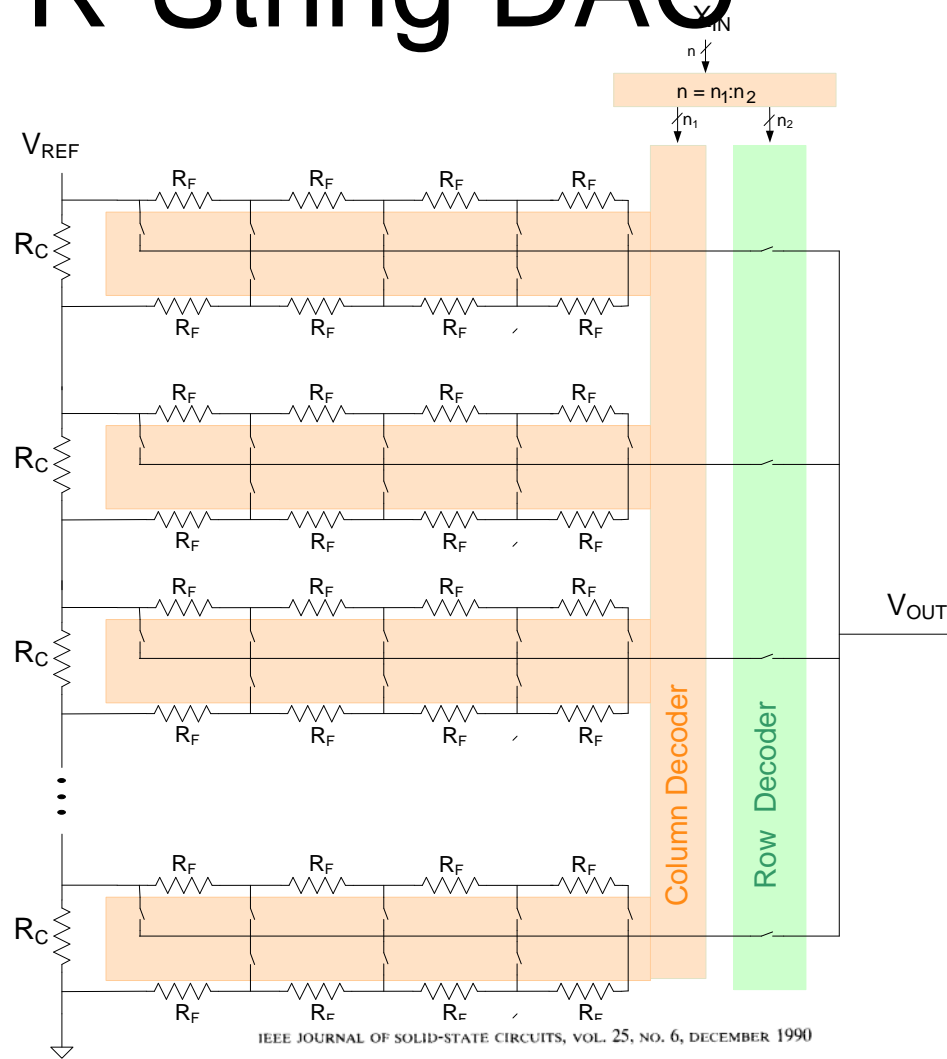# R-String DAC

R-String DAC

V_{IN}

$n = n_1 : n_2$

n_1 n_2

V_{REF}

R_F R_F R_F R_F

R_C

R_F R_F R_F R_F

R_F R_F R_F R_F

R_C

R_F R_F R_F R_F

R_F R_F R_F R_F

R_C

V_{OUT}

R_F R_F R_F R_F

R_F R_F R_F R_F

R_C

R_F R_F R_F R_F

Column Decoder

Row Decoder

Note Dual Ladder is used !

A 10-b 50-MHz CMOS D/A Converter
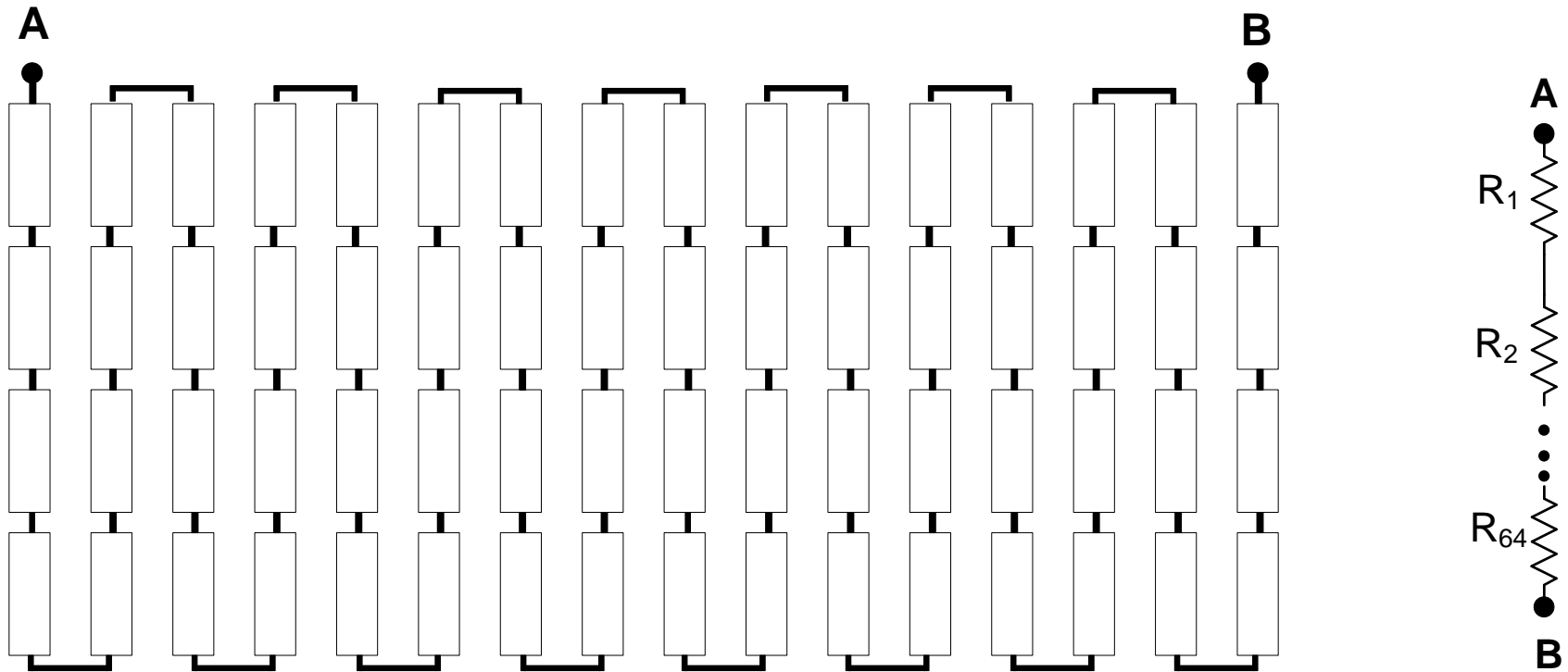with 75-Ω Buffer

MARCEL J. M. PELGROM, MEMBER, IEEE

Basic R-String DAC
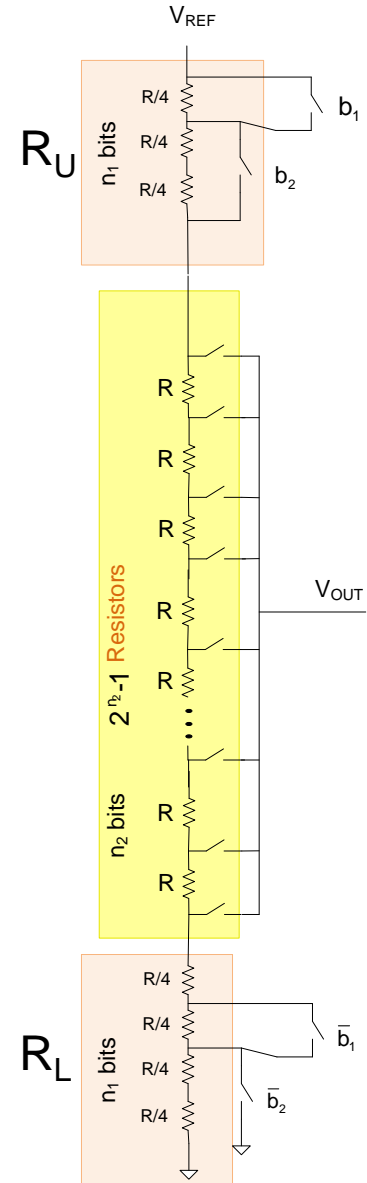
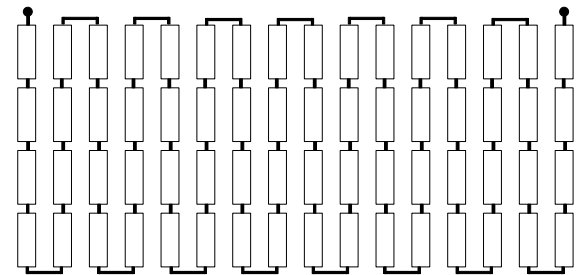
For all b_1 and b_2, $R_U + R_L = R$

- Another Segmented DAC structure

- Can be viewed as a "dither" DAC

- Often n_1 is much smaller than n_2

- Dither can be used in other applications as well

Resistor Layout

A   **B**
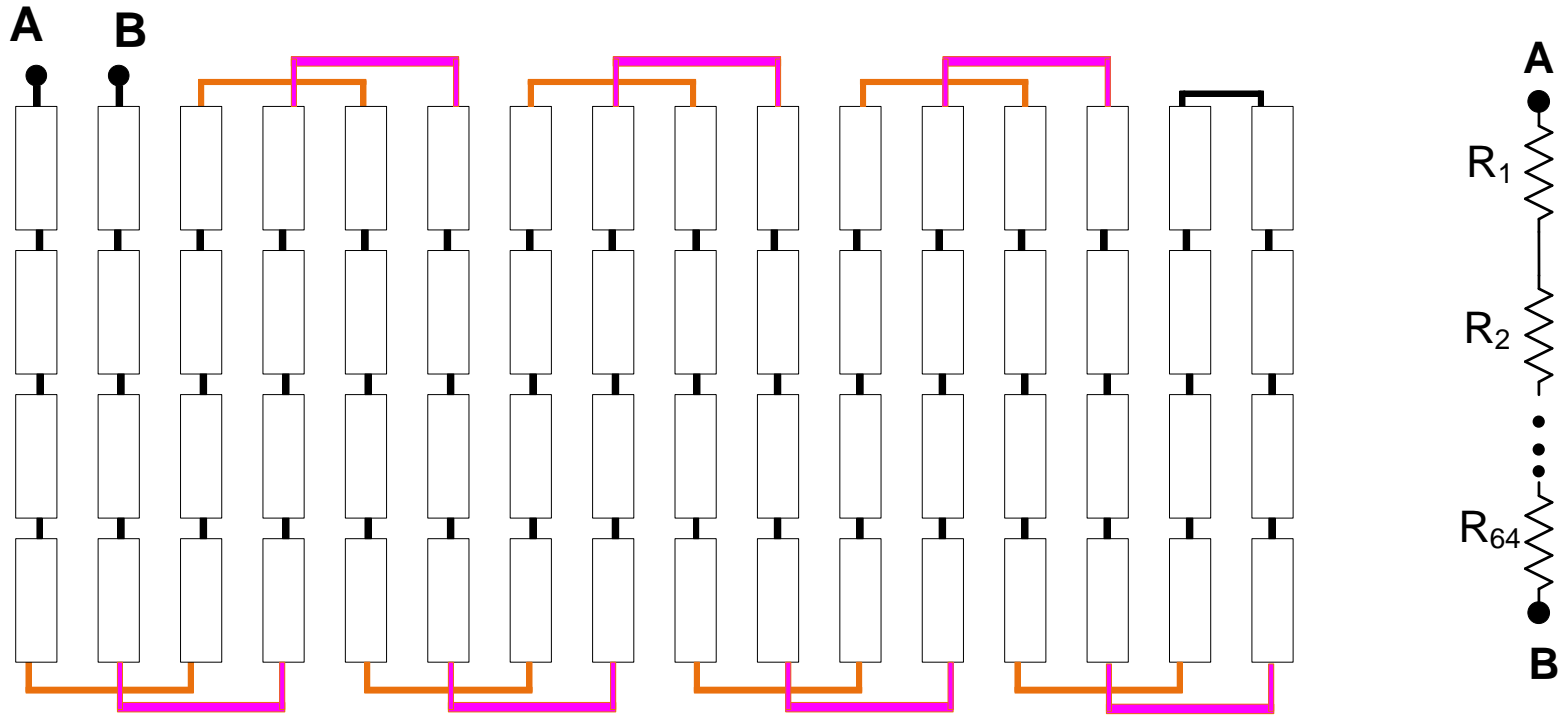
A

R_1

R_2

⋮

R_{64}

B

Standard Series Layout of 64 resistors
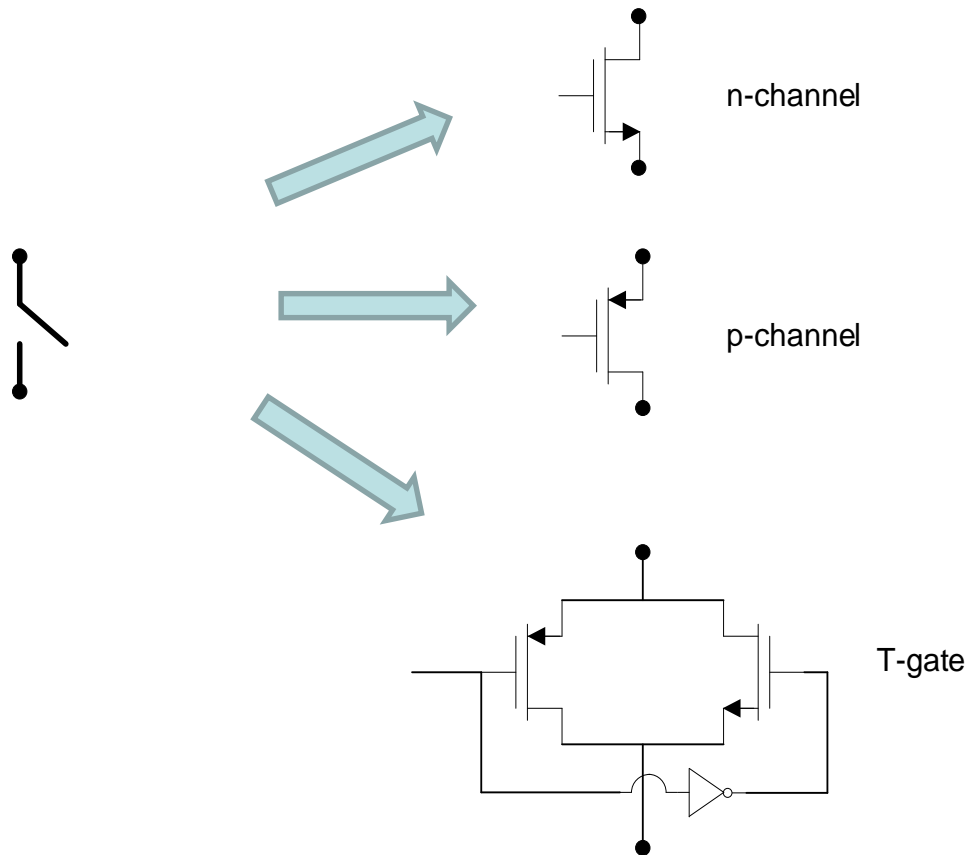
Resistor Layout

Correction on Terminology

Layout of 64 resistors with reduced gradient sensitivity
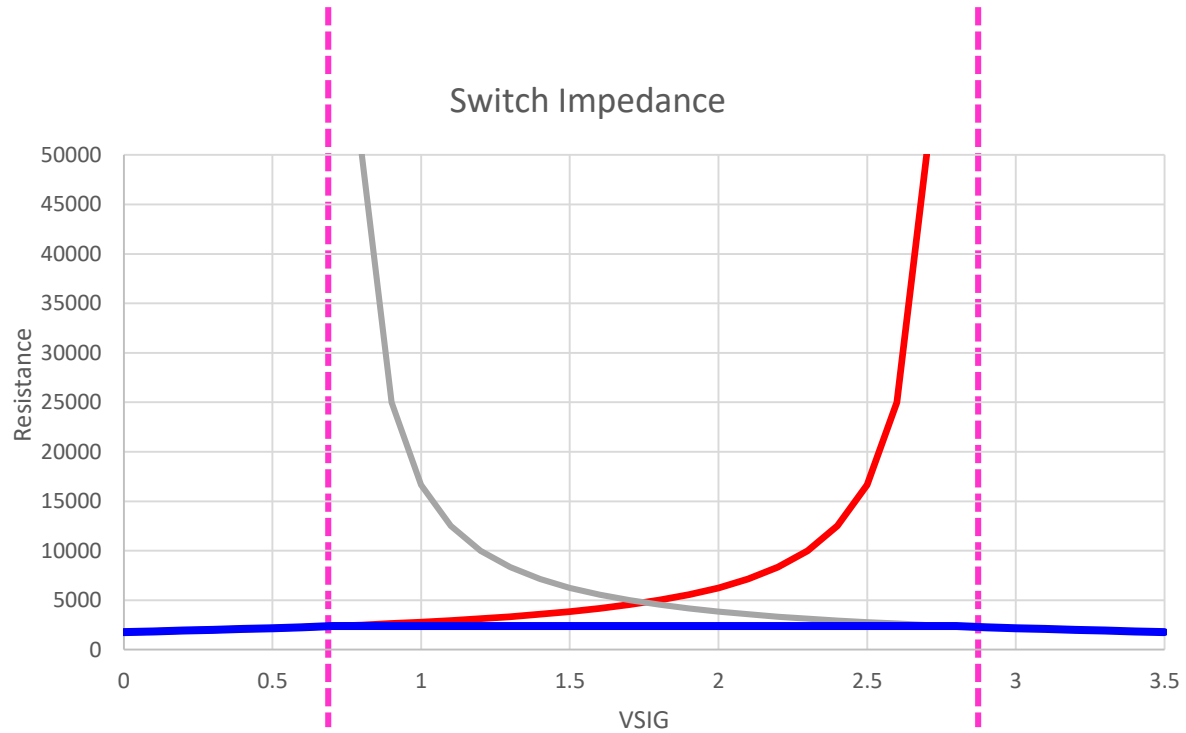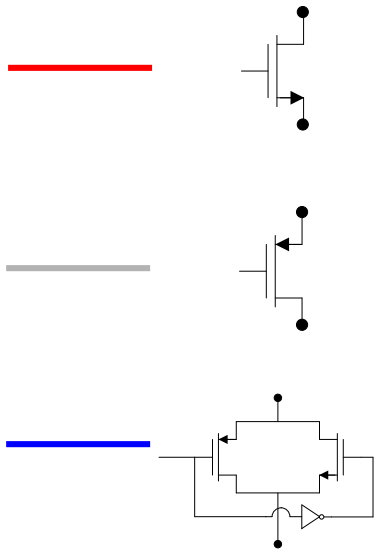
Switches used extensively in data converters !
Switch Implementation Issues
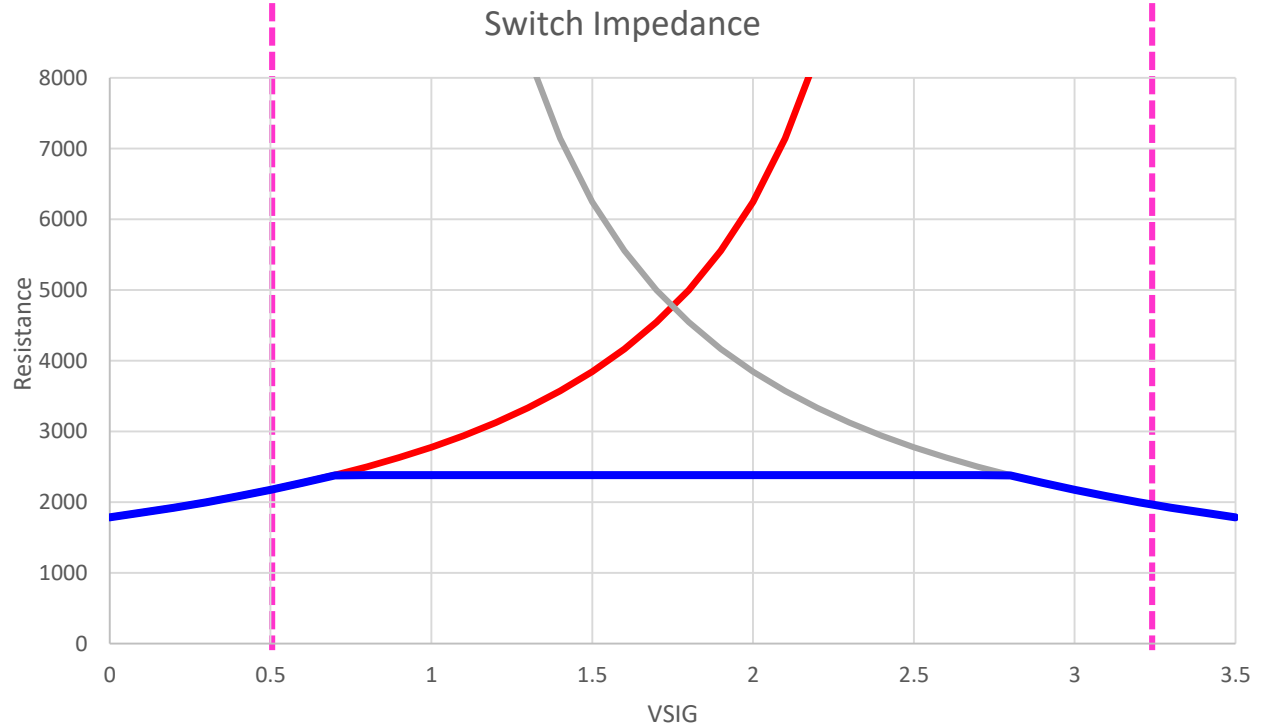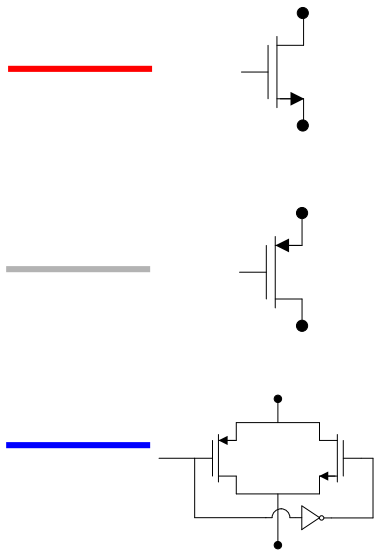
Basic Simple Switches
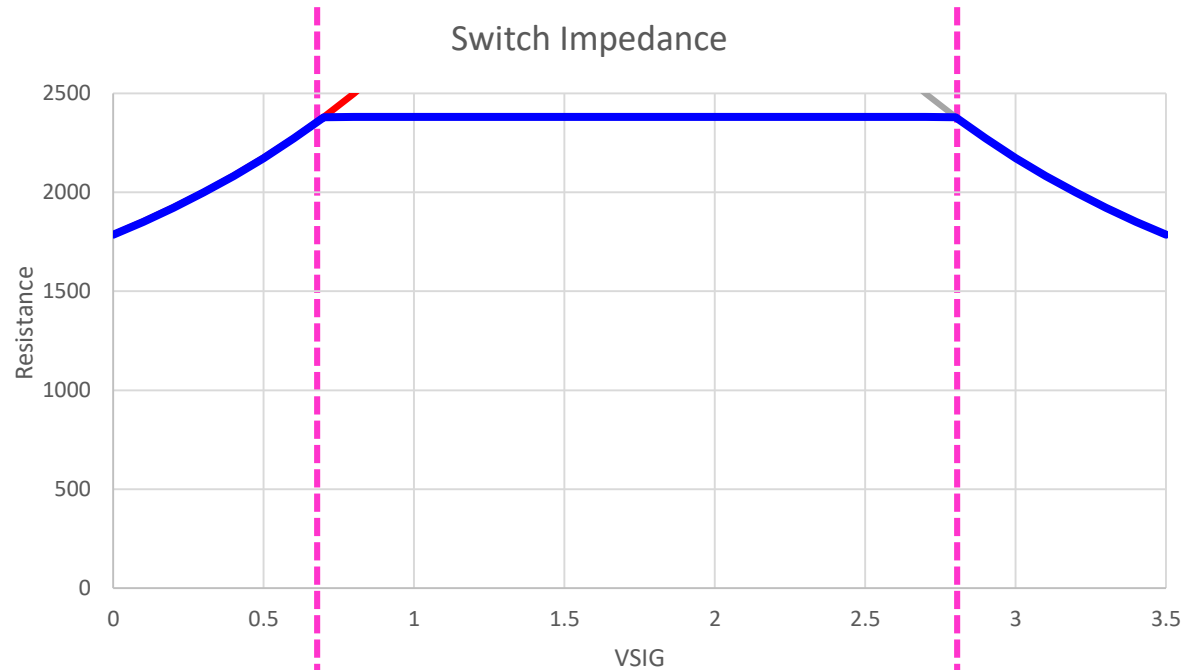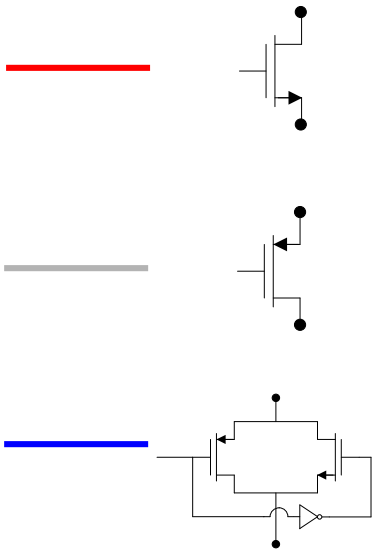
n-channel

p-channel

T-gate

Switch Implementation Issues

$V_{THn}=0.7$
$V_{THp}=-0.7$
$W_p=3W_n$
$L_p=L_n$
$V_{DD}=3.5V$

Switch Impedance

Switch Implementation Issues
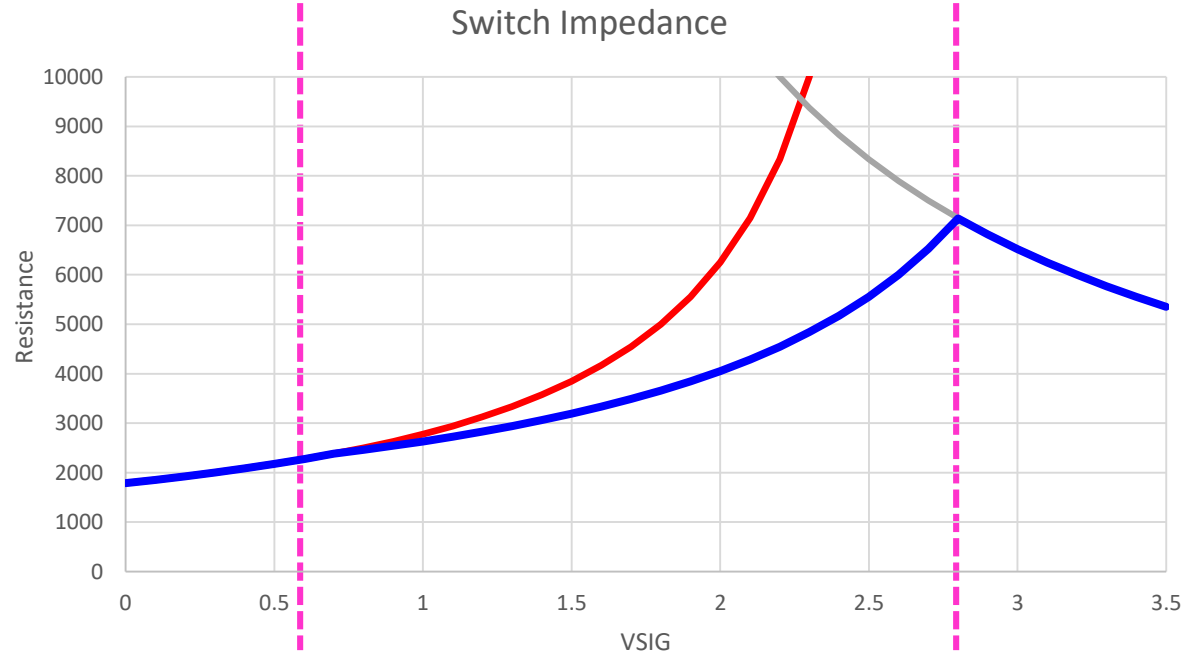
$V_{THn}=0.7$
$V_{THp}=-0.7$
$W_p=3W_n$
$L_p=L_n$
$V_{DD}=3.5V$

Switch Impedance

Switch Implementation Issues
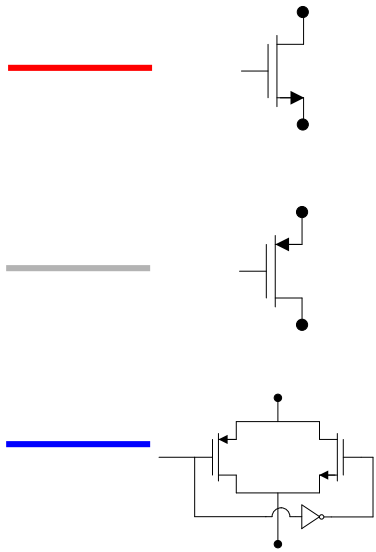
$V_{THn}=0.7$
$V_{THp}=-0.7$
$W_p=3W_n$
$L_p=L_n$
$V_{DD}=3.5V$

Transmission Gate Impedance Can be Reasonably constant
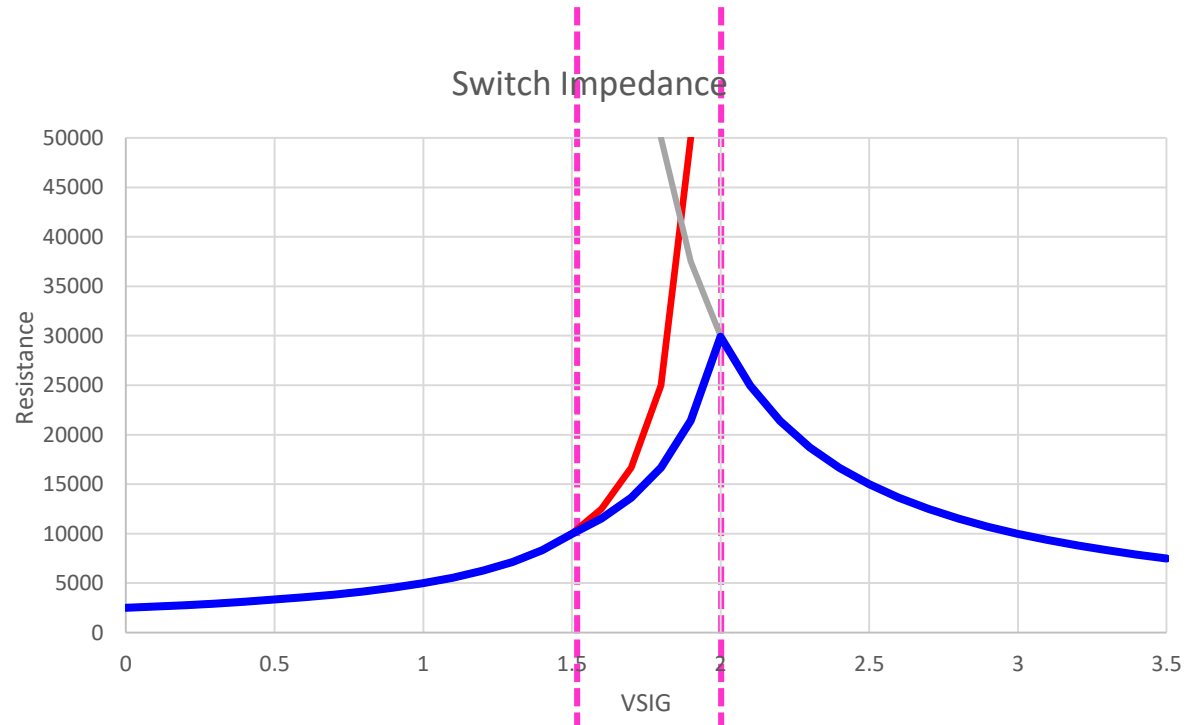
Switch Implementation Issues

$V_{THn}=0.7$
$V_{THp}=-0.7$
$W_p=W_n$
$L_p=L_n$
$V_{DD}=3.5V$

Equal-Sized Switches

Switch Impedance

Switch Implementation Issues

Equal-Sized Switches
High Threshold Voltages

$V_{THn}=1.50$
$V_{THp}=-1.5$
$W_p=W_n$
$L_p=L_n$
$V_{DD}=3.5V$

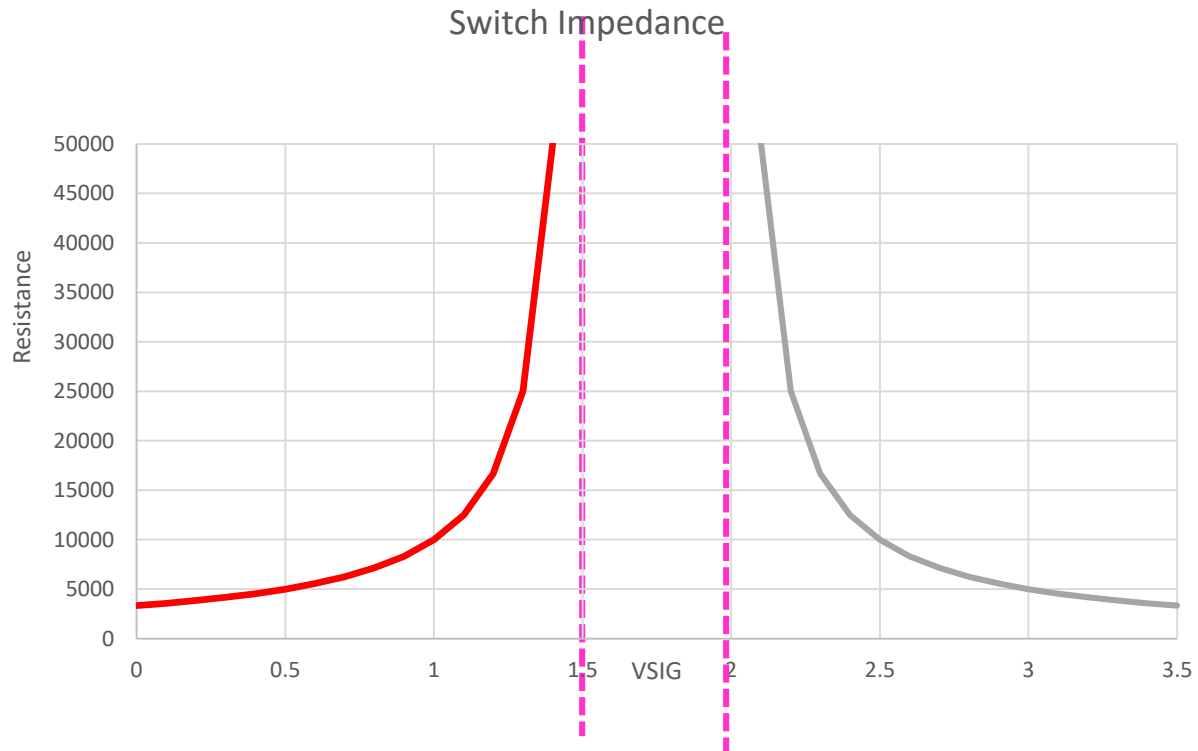Switch Impedance

Resistance

VSIG
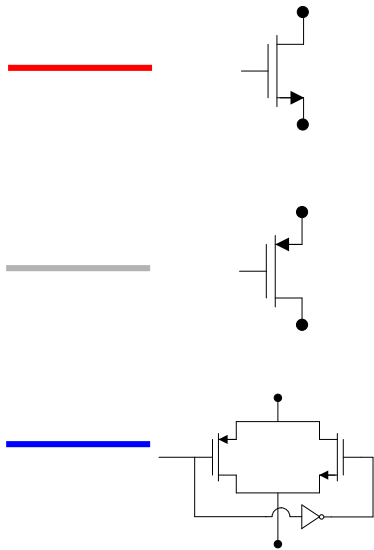
Even Transmission Gate Does Not Perform Well

Switch Implementation Issues

$V_{THn}=2.0$
$V_{THp}=-2.0$
$W_p=3W_n$
$L_p=L_n$
$V_{DD}=3.5V$

Tough unlikely, this is what would happen if very high threshold devices were used
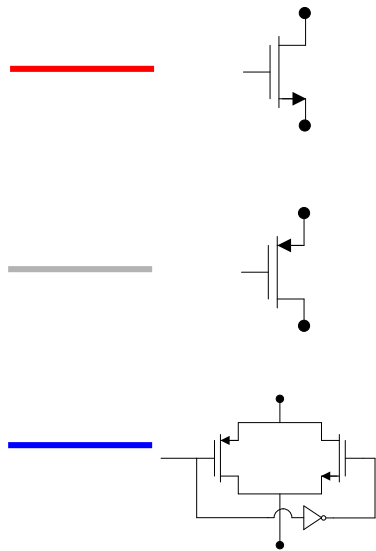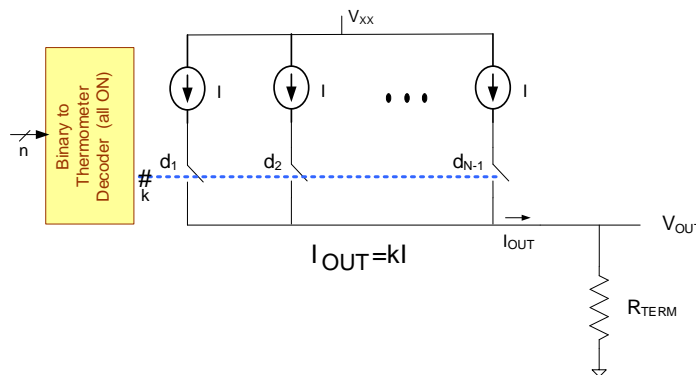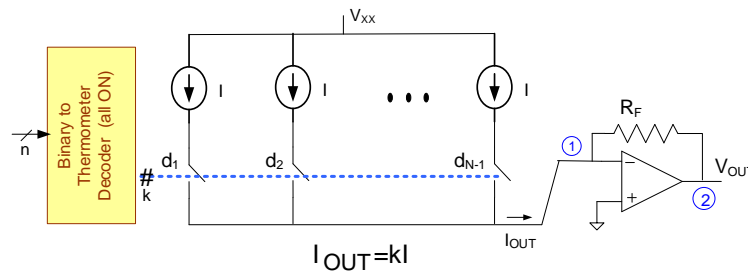
Gap where neither switch is working

Current Steering DACs

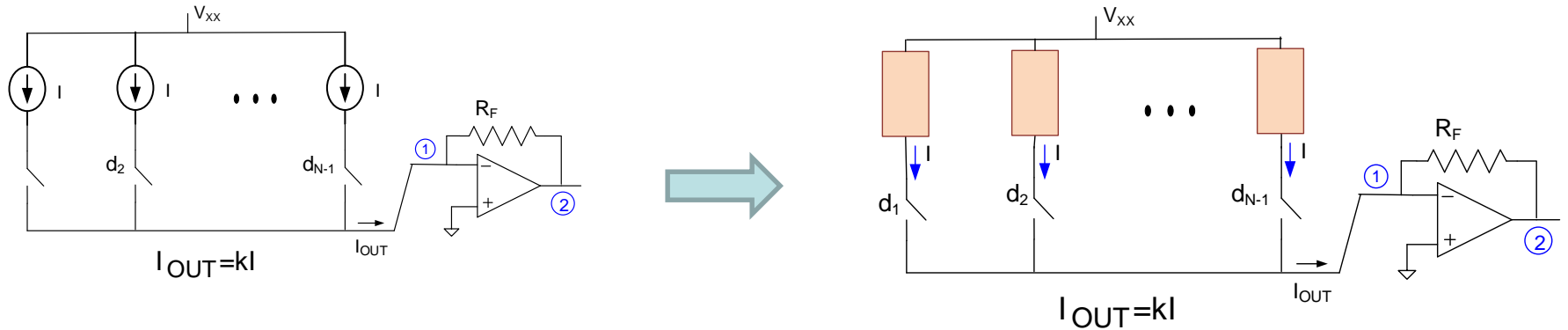Current will be "steered" to a resistive load (on chip)

Output could be a current (user supplies load)
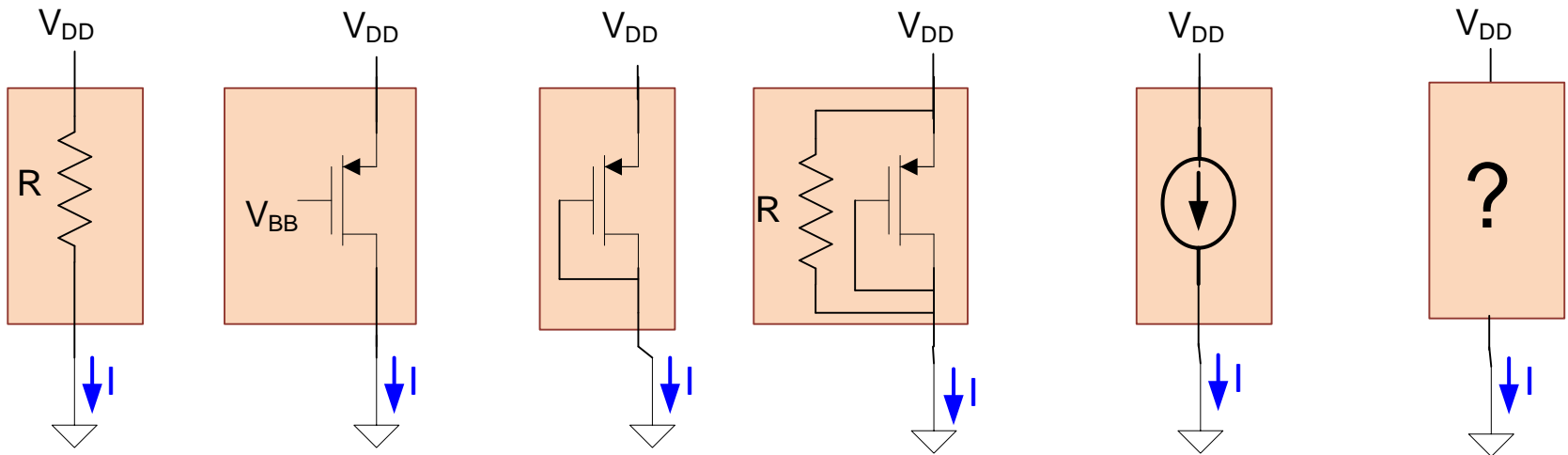
Basic Concept of Current Steering DACs
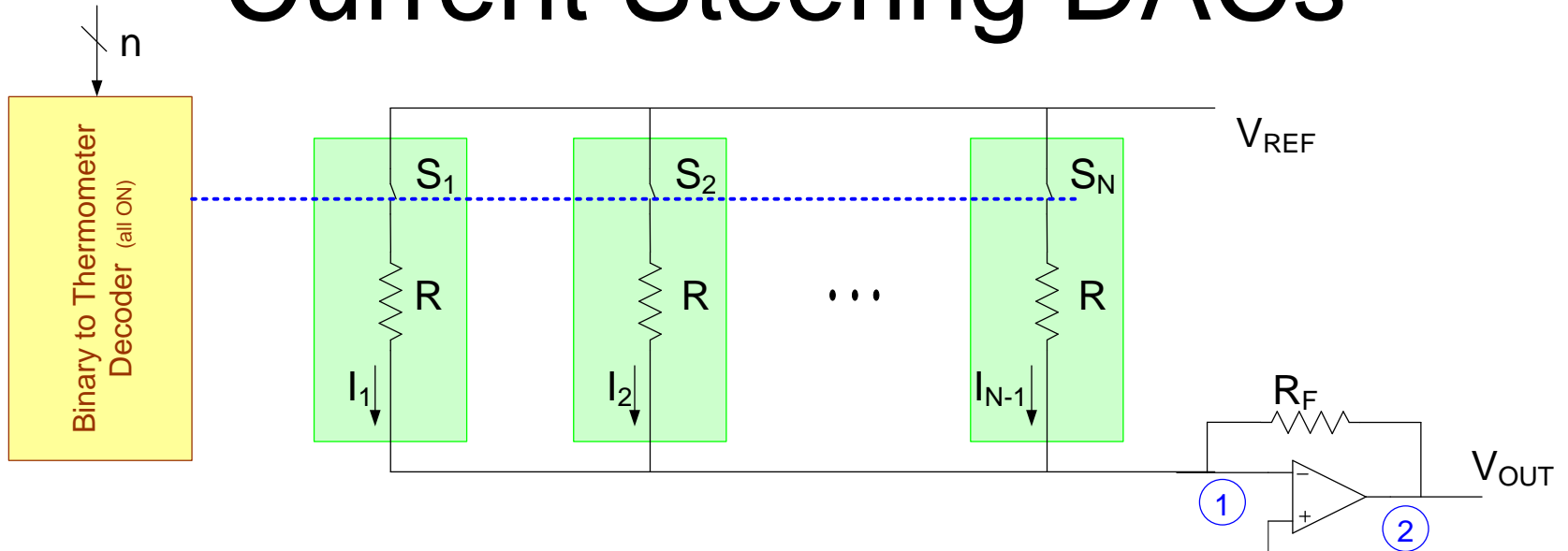
Current Steering DACs

What is important is the current generated, not whether it comes from a "current source"

Many potential current generator blocks, just require that all be ideally identical
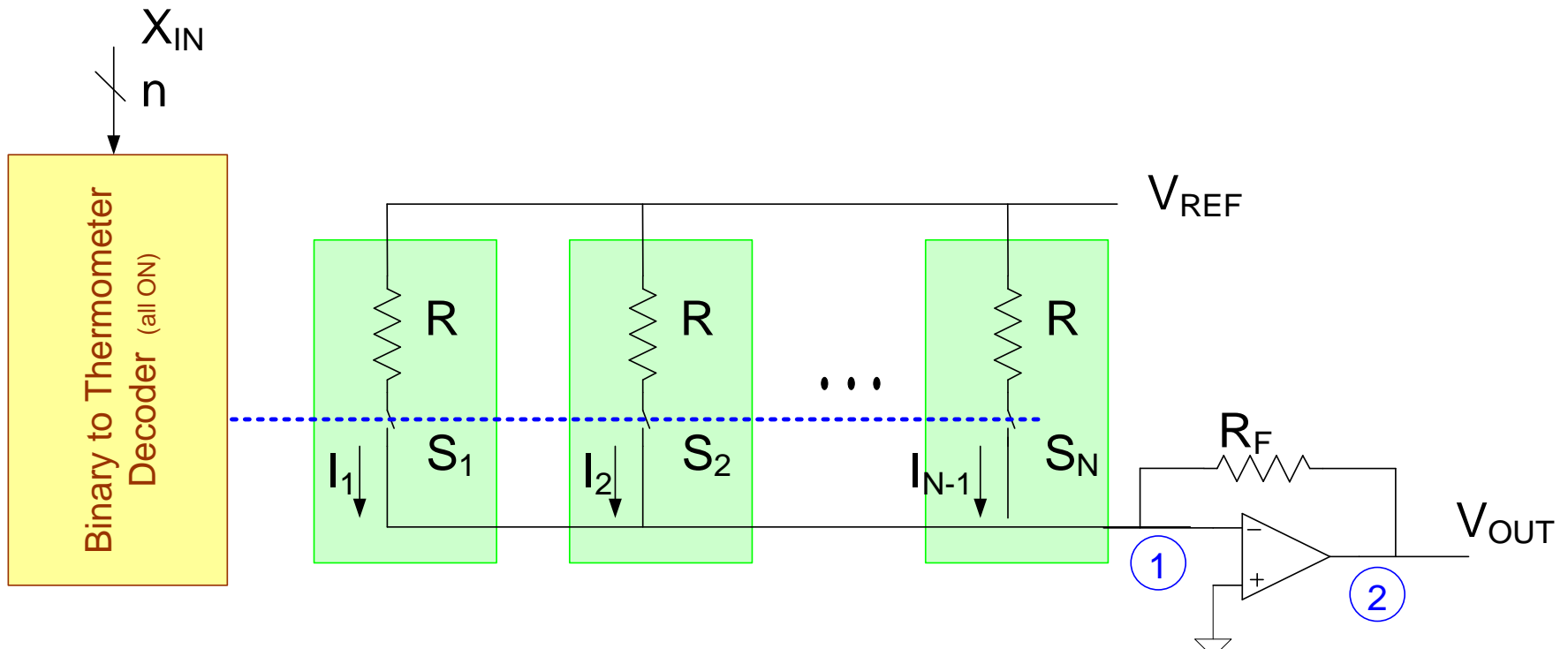
Current Steering DACs

Inherently Insensitive to Nonlinearities in Switches and Resistors

- Termed "top plate switching"
- Thermometer coding
- Excellent DNL properties
- INL may be poor, typically near mid range

- INL is a random variable with variance approximately proportional to area $\sigma = \dfrac{A_{PEL}}{\sqrt{A}}$
- Area gets large for good yield with large n

- Each additional bit of resolution requires a factor of 2 increase in area if same sized resistors are used
- Each additional bit of resolution requires another factor of 4 increase in area to maintain the same yield
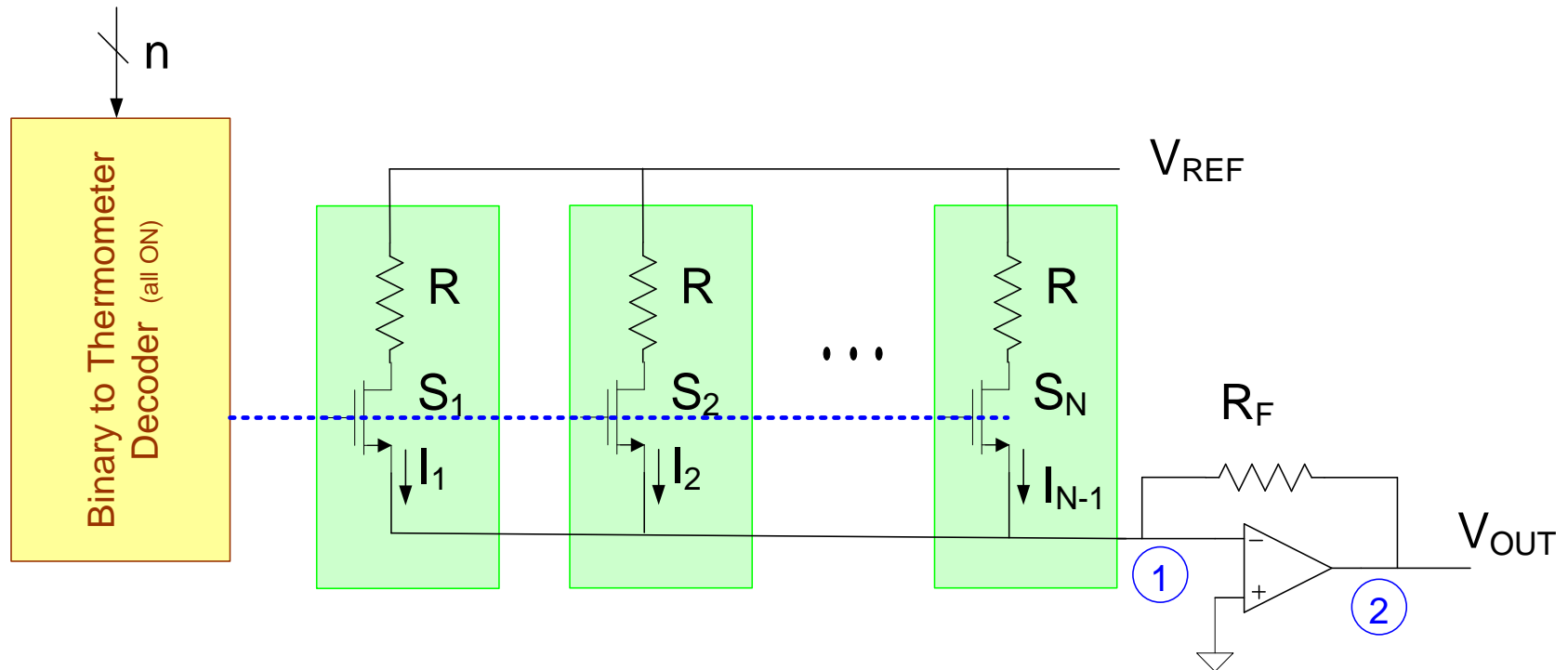
Current Steering DACs

Inherently Insensitive to Nonlinearities in Switches and Resistors
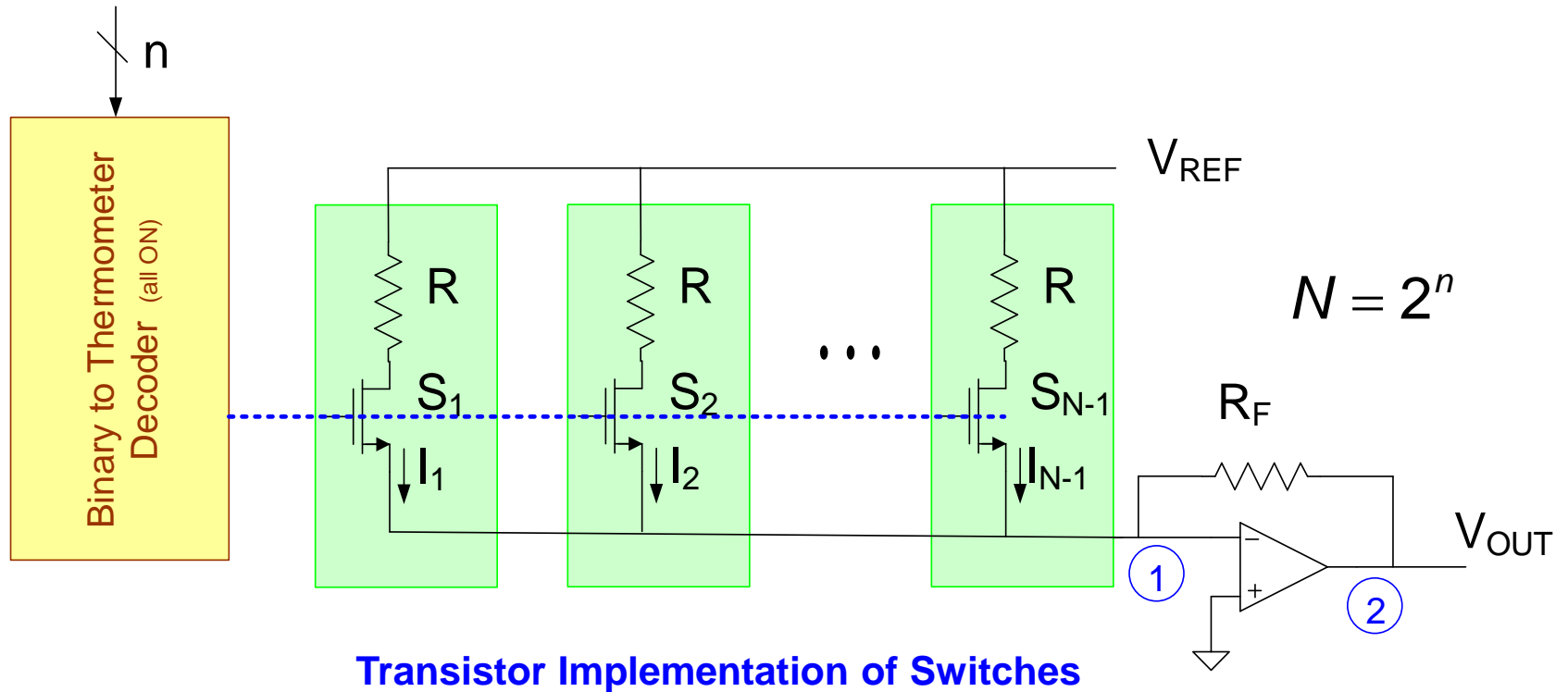**Smaller ON resistance and less phase-shift from clock edges**

- Termed "bottom plate switching"
- Thermometer coded

Current Steering DACs

Transistor Implementation of Switches

Current Steering DACs

Transistor Implementation of Switches

How should the op amp be compensated?
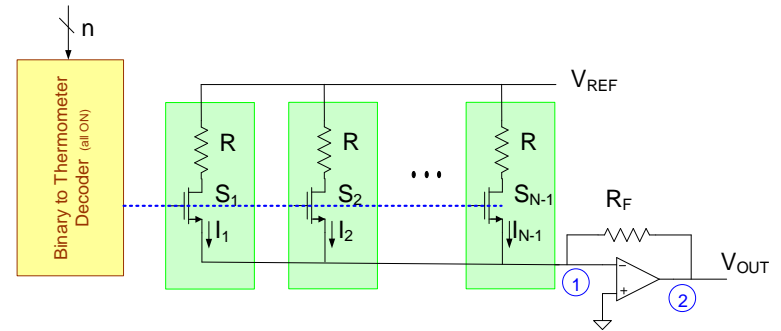
Assume k switches are on   0<k<N-1

$$\beta = \frac{\dfrac{R_{CELL}}{k}}{\dfrac{R_{CELL}}{k}+R_F} = \frac{R_{CELL}}{R_{CELL}+kR_F}$$

If $V_{OUTFS} = V_{REF}$ $R_{CELL} = NR_F$

$$0.5 < \beta \le 1$$

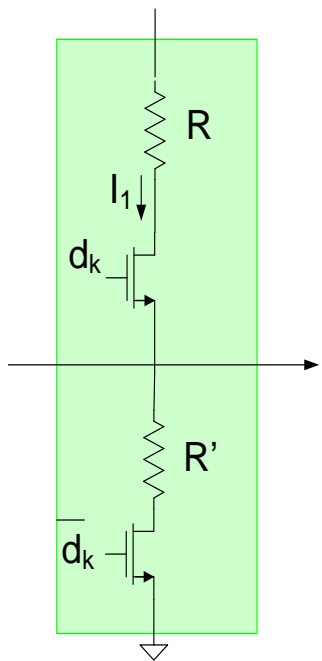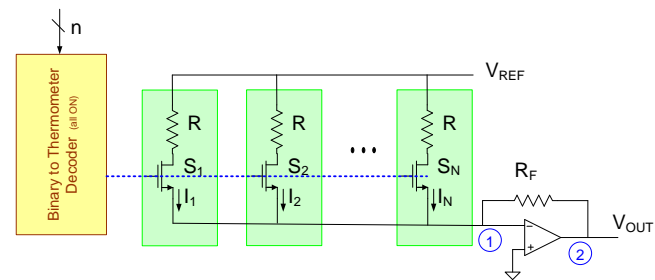$N = 2^n$

How should the op amp be compensated?

$$\beta = \dfrac{\dfrac{R_{CELL}}{k}}{\dfrac{R_{CELL}}{k} + R_F} = \dfrac{R_{CELL}}{R_{CELL} + kR_F}$$

$$V_{OUTFS} = V_{REF} \qquad 0.5 < \beta \leq 1$$

Current Steering DACs
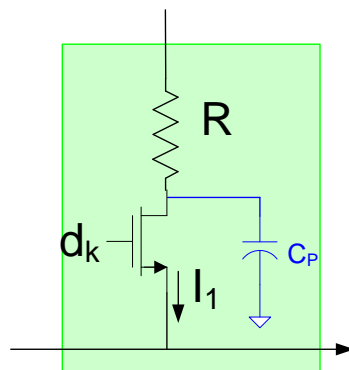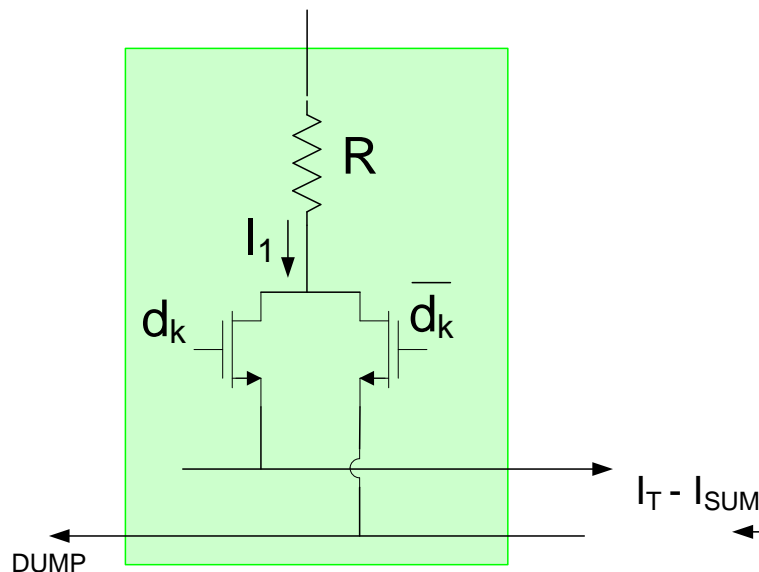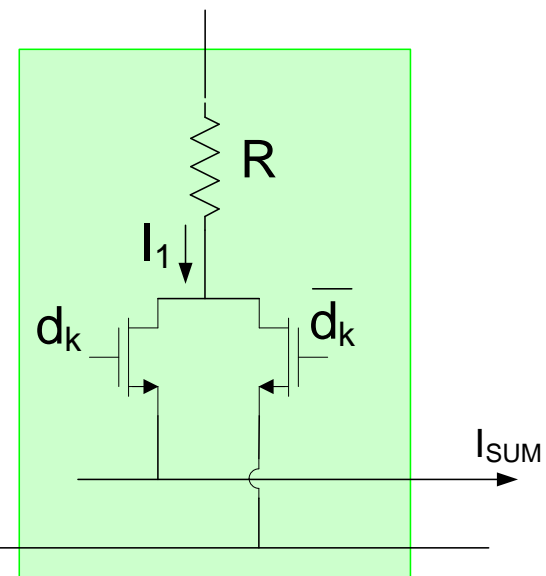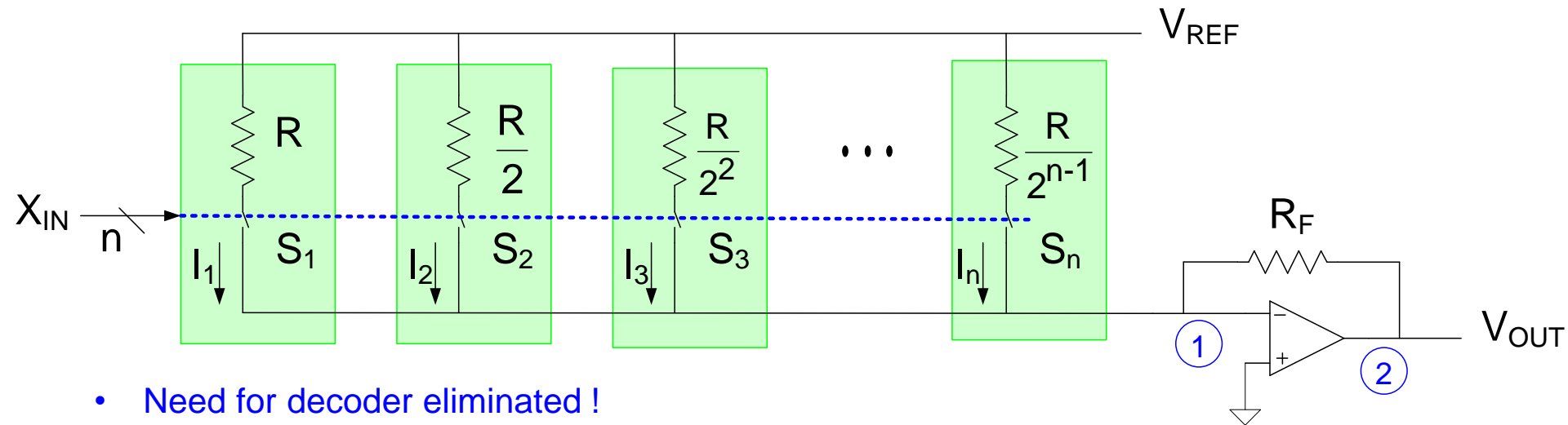

β Compensation

C_P Compensation

Differential Output

Current Steering DACs

Binary-Weighted Resistor Arrays

- Need for decoder eliminated !
- DNL may be a major problem
- INL performance about same as thermometer coded if same unit resistors used
- Sizing and layout of switches is critical
- Unary resistor arrays usually used with common-centroid layout(at least for MSB)
- Ratio matching strongly dependent upon area (if common-centroid used to eliminate gradients)
- INL is a random variable with variance approximately proportional to $\sigma = \dfrac{A_{PEL}}{\sqrt{A}}$
- Area gets large for good yield with large n

Observe thermometer coding and binary weighted both offer some major advantages and some major limitations

Current Steering DACs
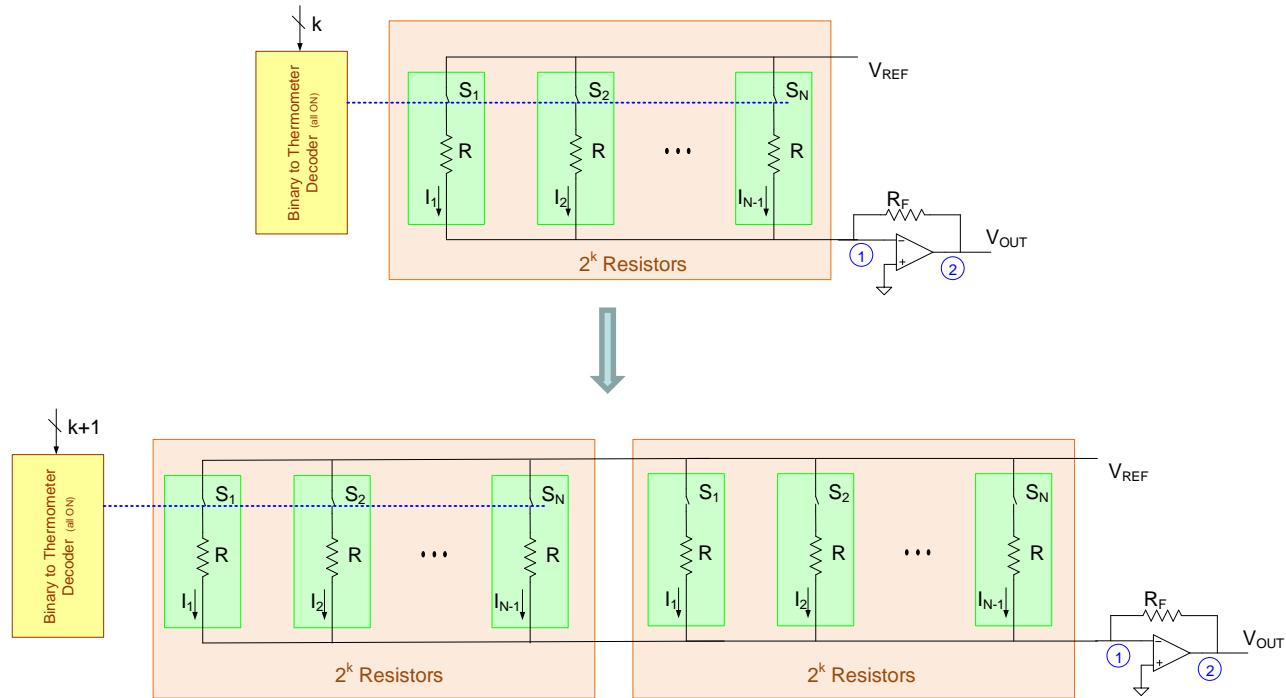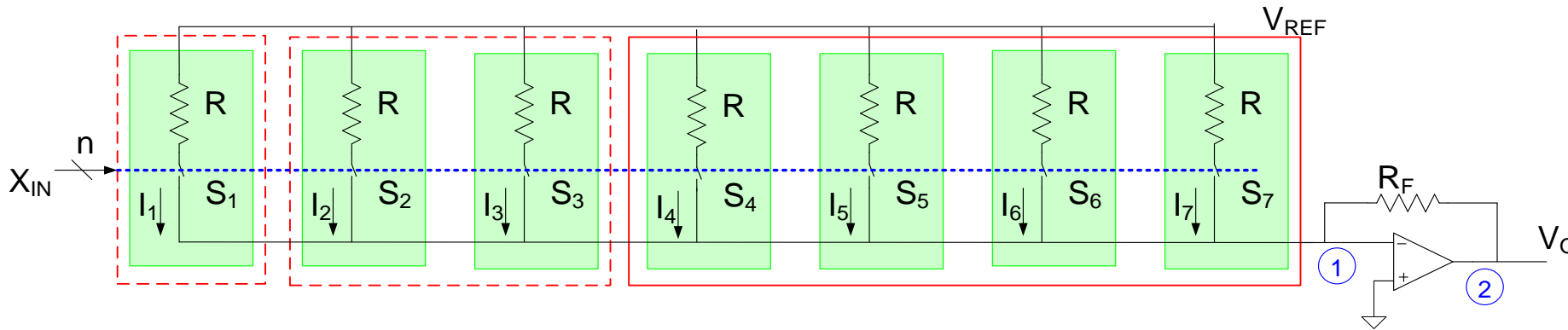

INL may be poor, typically near mid range

approximately $\sigma = \dfrac{A_{PEL}}{\sqrt{A}}$

Consider a k-bit structure that has an acceptable (and desired) yield of Y

Can a k+1 bit structure be easily implemented by simply making 2 copies of the resistor array and adding one bit to the decoder?

The one-afternoon design ?
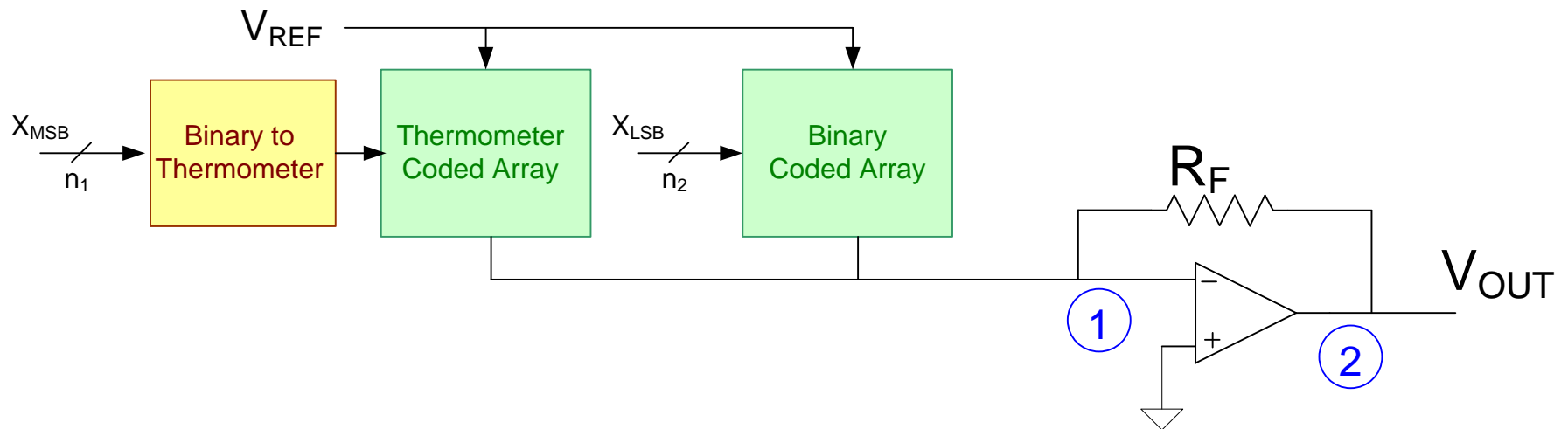
Current Steering DACs

Binary-Weighted Resistor Arrays

Actual layout of resistors is very important

As stated earlier, bundled unary cells are almost always used

Current Steering DACs

Segmented Resistor Arrays

- Combines two types of architectures
- Inherits advantages of both thermometer and binary approach
- Minimizes limitations of both thermometer and binary approach

Stay Safe and Stay Healthy !

End of Lecture 32